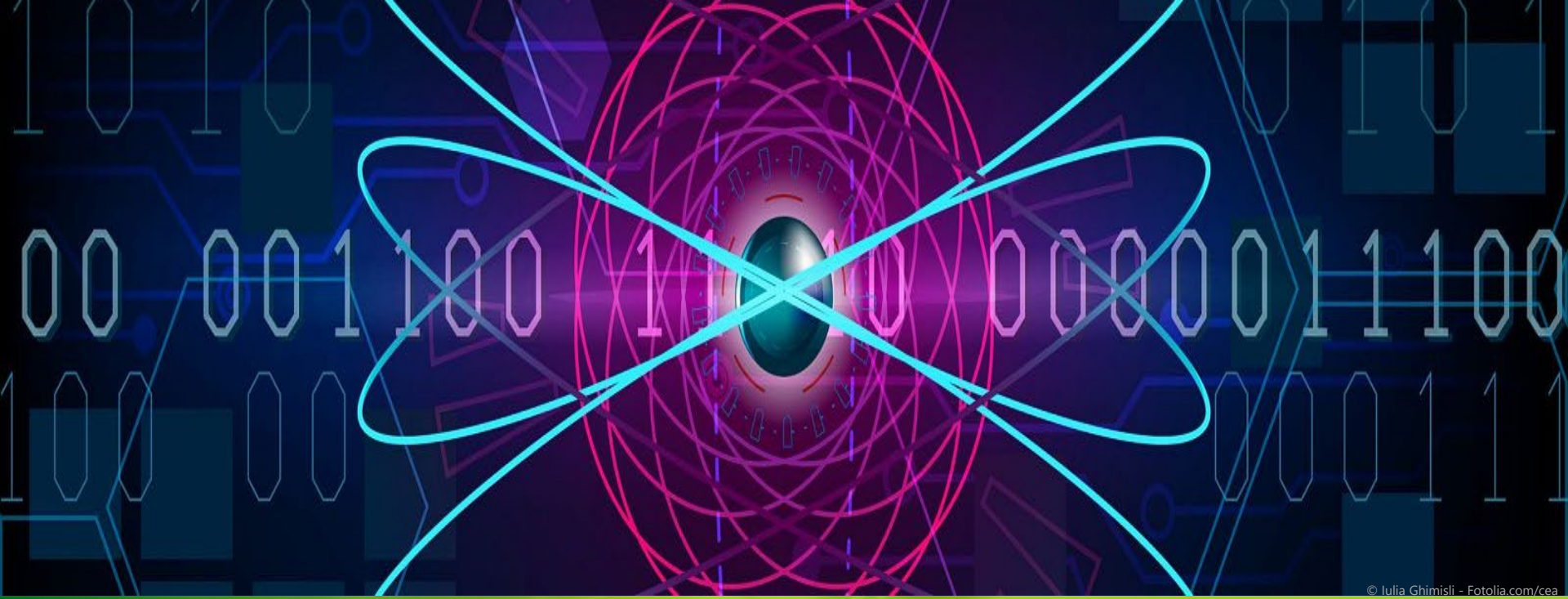


SILICON BASED QUANTUM COMPUTING

leti
cea tech

irig

QuantumSilicon
Grenoble

UNIVERSITÉ
Grenoble
Alpes

NÉEL
institut

WHO WE ARE

Access to platforms

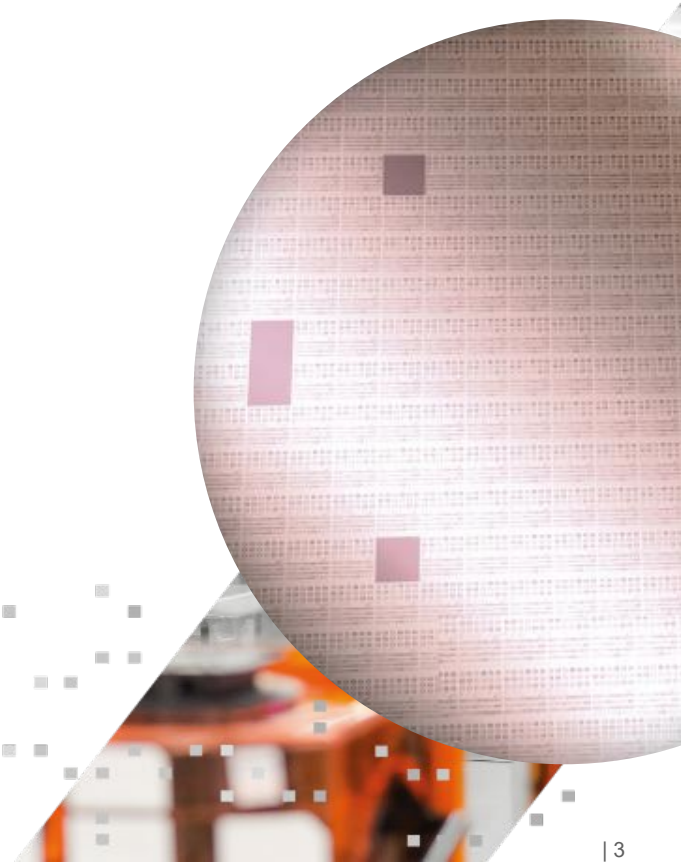
nanocaracterisation / 200 & 300 mm Si / analog & rf IC design / (LT) probe stations / cryogeny / simulation & modeling / low level software development / …

OUR GOAL

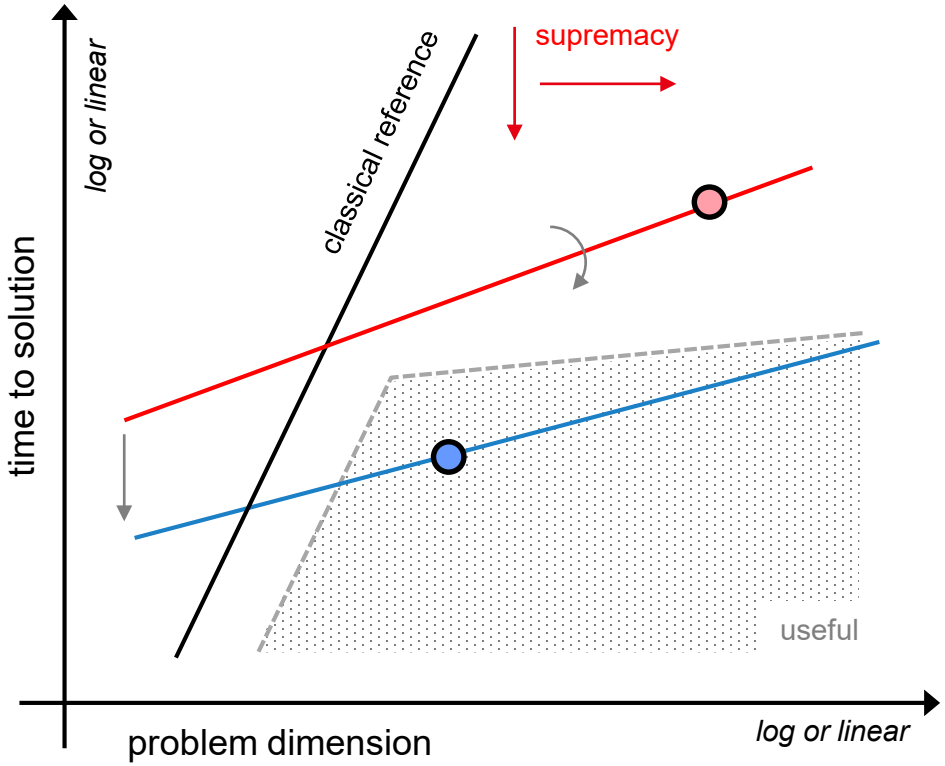
Open the path

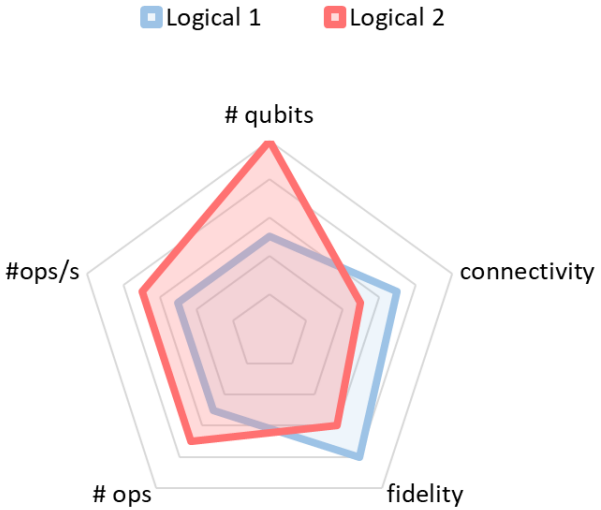
to Scalable Quantum Accelerator

to Solve Useful Problems



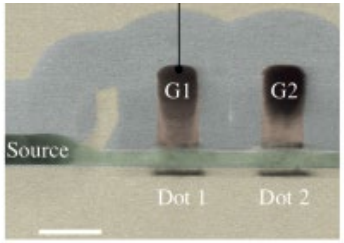
SOLVING PROBLEMS



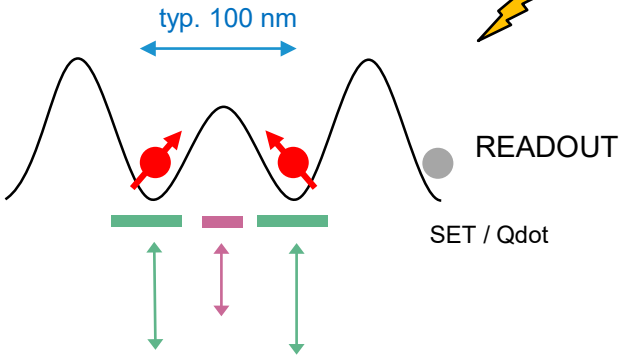


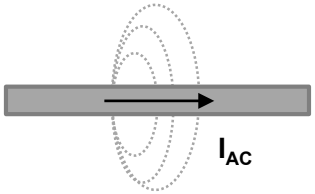
SEMICONDUCTOR SPIN QUBITS IN 1 SLIDE

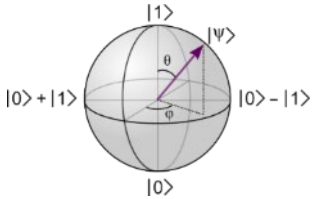
Gate defined quantum dots + $\vec{B}$ ⟶ Spin degree of freedom of (an) electrons

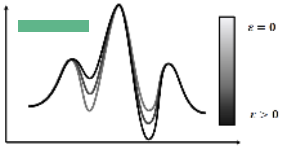


Wide-spacer CMOS quantum dots using SET

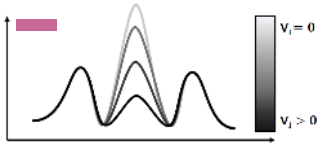




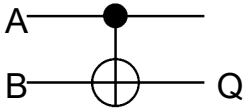




*effect of detuning **



*effect of exchange gate **



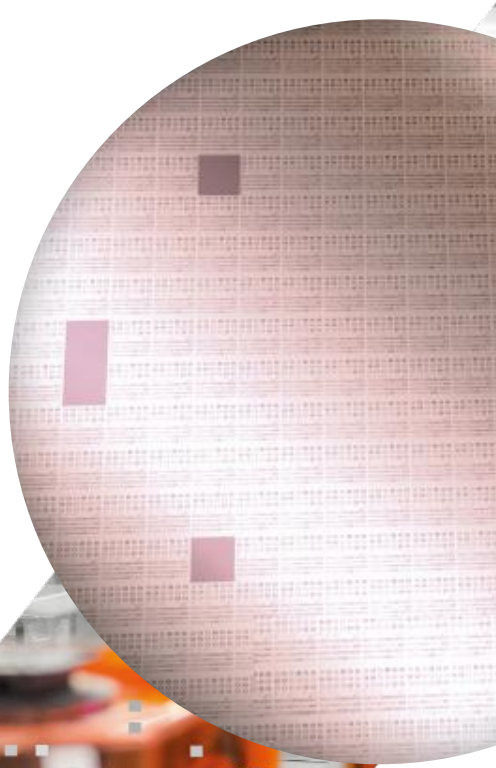
SI TOOLBOX

typical spacing of 100 nm

10^6 qubits in 100 µm x 100 µm

Integration of discrete components (form factor reduction & SNR improvement)
Better interface control
Better thickness control
Better chemical composition control
Better critical dimensions control

thanks to VLSI technology

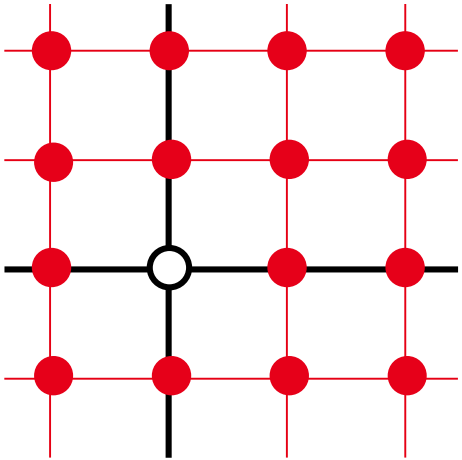


LEVERAGING SI SPIN QUBITS SCALABILITY

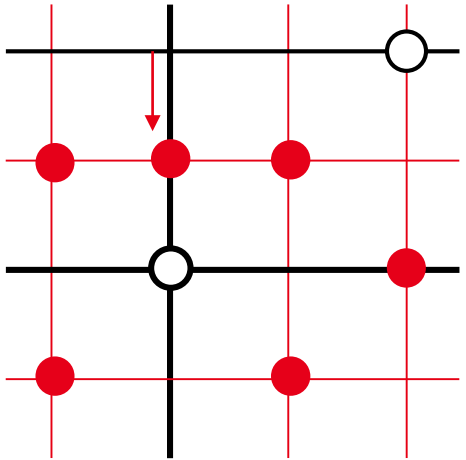
typical spacing of 100 nm

10^6 qubits in 100 µm x 100 µm

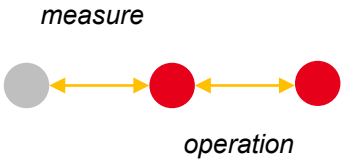
2n wires
n^2 qubits

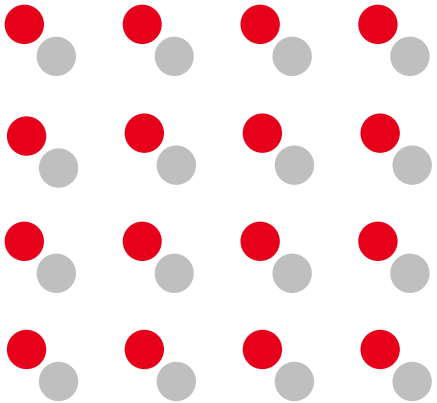


cross bar like solution



parallel operations

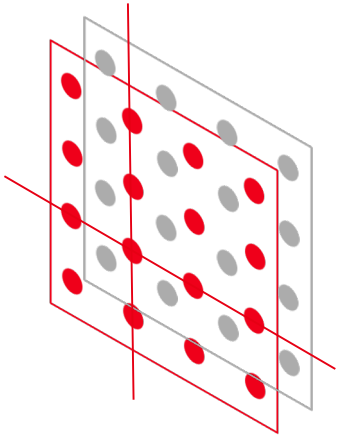


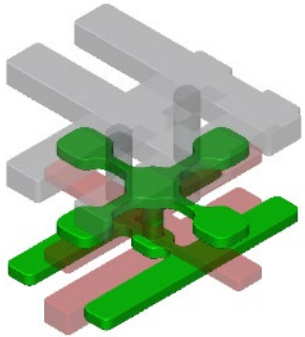


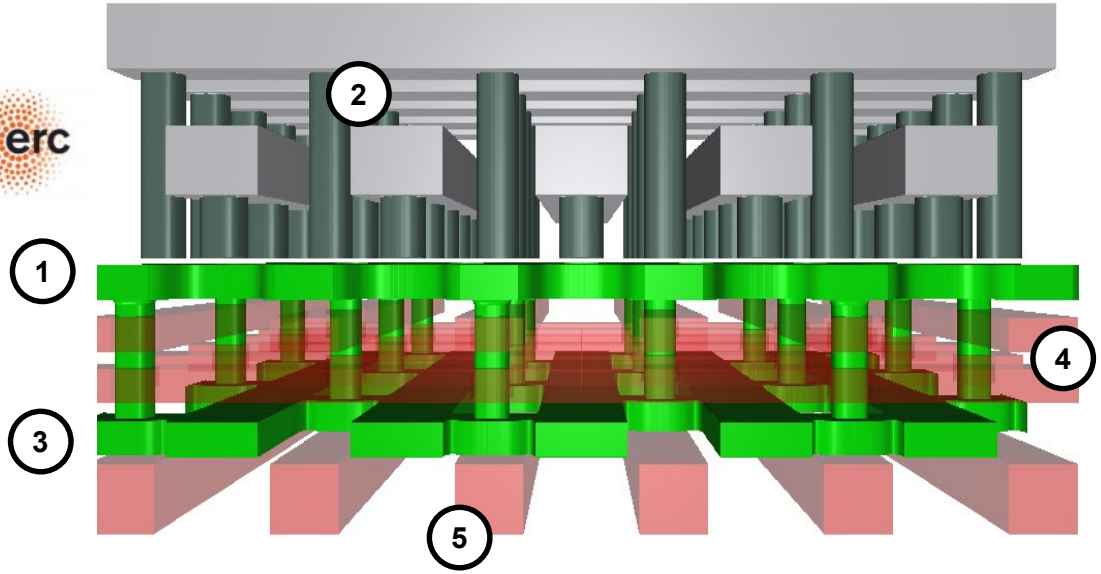
intricated networks

adapted from Ruoyu et al., DOI: 10.1126/sciadv.aar3960

3D DESIGN SOLUTION

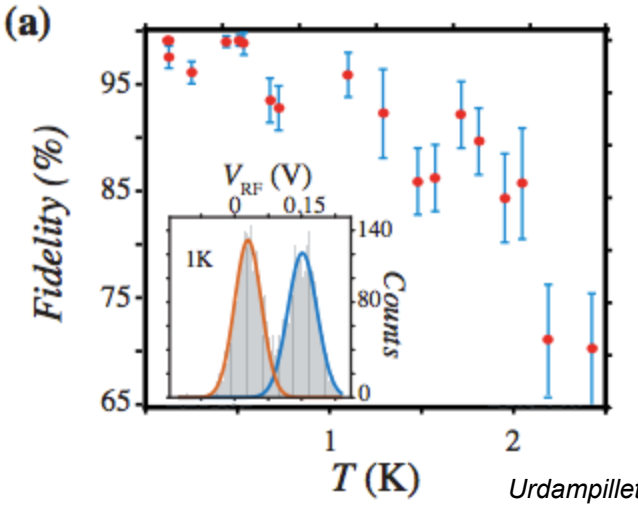






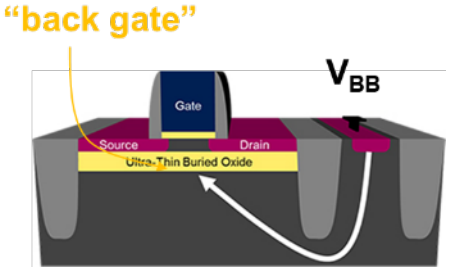
Meunier, De Franceschi, Vinet, Hutin (2017)

CRYOGENIC ELECTRONIC



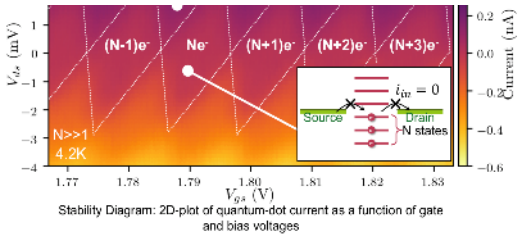
Urdampilleta et al., arXiv:1809.04584

T° of operation	Typical cooling power
20mK	30µW
100mK	1mW
1K	100mW-1W



FDSOI Cryo CMOS

More to come @ISSCC'2020

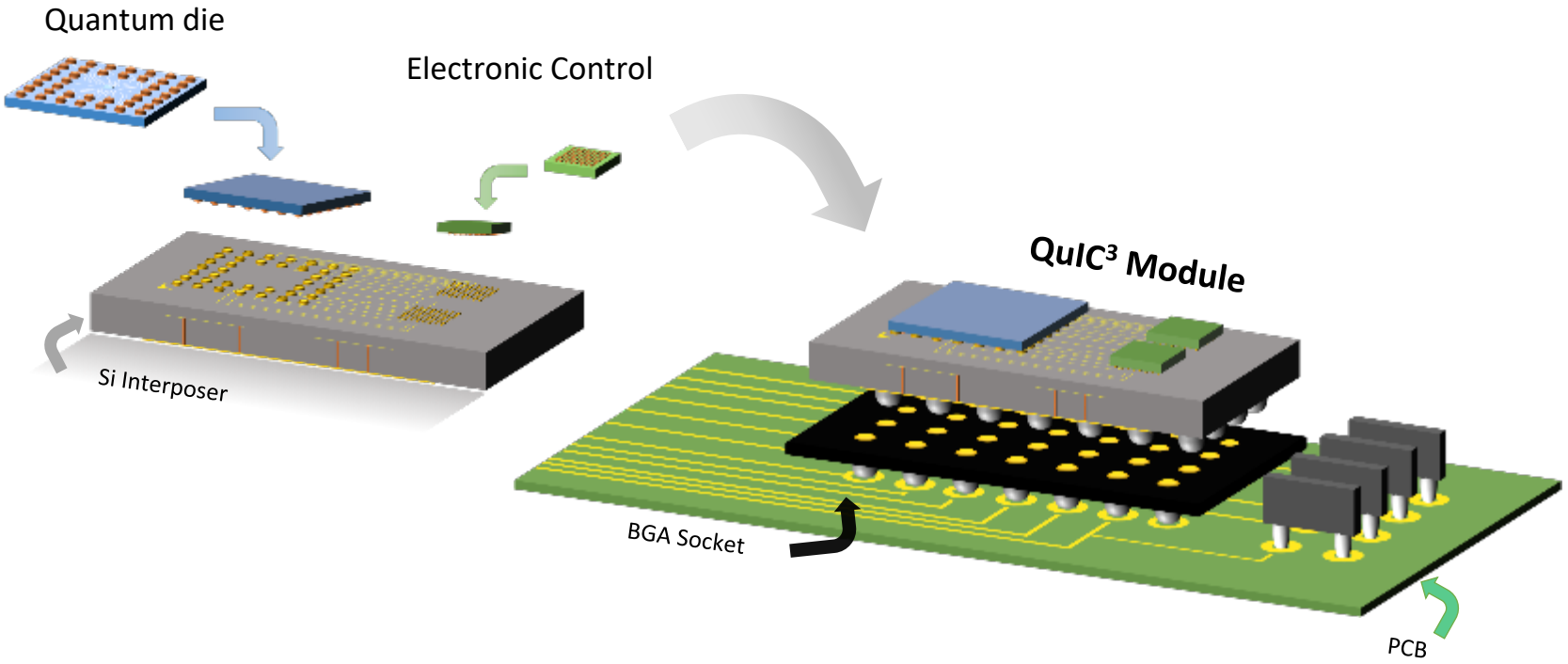


Stability Diagram: 2D-plot of quantum-dot current as a function of gate and bias voltages

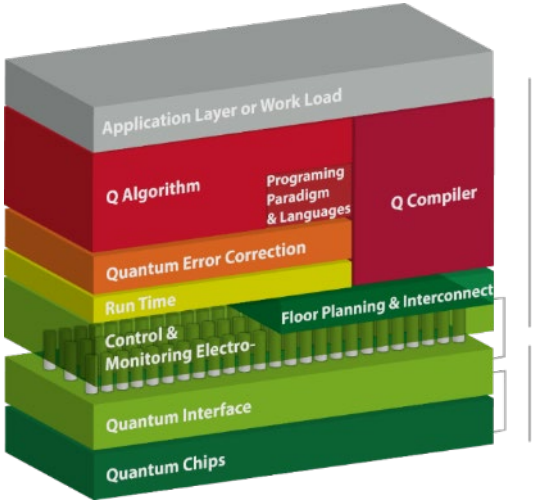
Quantum parameter extraction with our cryo control circuits

# of MOS ~ between 2 and 20 millions digital MOS @ full activity @ 1K

CRYOGENIC INTEGRATION



FULL OVERVIEW

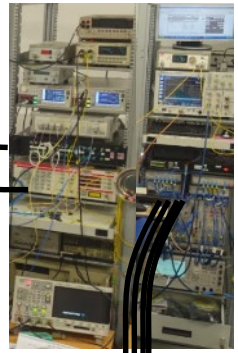


Room Temperature

Cryo

Run-time SW and algorithms

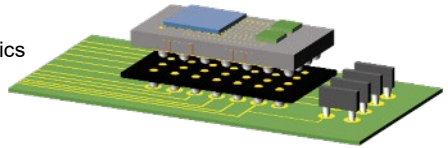
Lab equipment



HW drivers

Qubit array & fanout

Control electronics as Interposer



PCB substrate

Cryostat

CONCLUSION

Si spin qubit in CMOS geometry

2D array with control procedure

Vision for large scale architecture

Path defined with applicability as a driver

Still a long way to go… but a good roadmap !